UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,561	01/22/2004	Christopher A. Menkus	08211/0200350-US0/P05787	4900

38845 7590 04/26/2006

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,561	MENKUS ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application is in response to communication filed on 1/22/04. Claims 1 – 20 are pending on this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bult U.S. patent No. 6,100,836.

Regarding claim 1, Fig. 5 of Bult discloses a circuit for reducing the current density on a bus (buses on 62a) coupled to a plurality of circuits (Fig. 6 discloses plurality amplifier circuit, the circuit comprising: a first amplifier circuit (40) of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current (output current of 40) for the bus; and a first current source circuit (54) that is arranged to provide a first local current (54) at an output of the first amplifier circuit (output node of 40) such that at least a portion of the first output current (output current of 40) is prevented from being carried on the bus (this is inherent to Fig. 5 of Bult, because the output current of 40 is split at the output node of 40).

Regarding claim 2, Fig. 5 further comprising a load circuit (60a) that is coupled to the bus.

Regarding claim 3, wherein the first amplifier circuit (40) is configured to provide the first output current to the bus in response to a first input voltage signal (voltage input at the gate of 40), and wherein the first output current is a differential current (current output of 40 is a differential current respect the output current of 42), and the first input voltage signal is a differential voltage signal (See Fig. 6 Vin+/Vin-).

Regarding claim 4, Fig. 5 further comprising: a second amplifier circuit (Second 40) of the plurality of circuits, wherein the second amplifier circuit is configured to provide a second output current (output current of second 40) for the bus.

Regarding claim 5, further comprising: a second current source circuit (second current source 54) that is configured to provide a second local current (second current 54) at an output of the second amplifier circuit (output current of second amplifier 40 such that at least a portion of the second output current is prevented from being carried on the bus (this is inherent to Fig. 5 of Bult, because the output current of 40 is split at the output node of 40).

Regarding claim 6, further comprising: a third amplifier circuit (third 40) of the plurality of circuits, wherein the third amplifier circuit is configured to provide a third output current to the bus (output current of the third 40); and a third current source (third current 54) circuit that is configured to provide a third local current (third current 54) at an output of the third amplifier circuit.

Regarding claim 7, wherein one of the amplifier circuits in the plurality of circuits is not saturated (first 40), and each of the other amplifier circuits (second, third of 40) in the plurality of circuits is saturated.

Regarding claim 8, Fig. 5 further comprising another bus (62a bus) that is coupled to another plurality of circuits (42's); another amplifier circuit (42) of the other plurality of circuits, wherein the other amplifier circuit (42) is configured to provide another output current (output current of 42) for the other bus; and another current source circuit (56) that is arranged to provide another local current (current 56) at an output of the other amplifier circuit (connection Node) such that at least a portion of the other output current is prevented from being carried on the other bus (this is inherent to Fig. 5 of Bult, because the output current of 40 is split at the output node of 40).

Regarding claim 9, wherein the first amplifier circuit includes'.
a first differential pair (40,42); and a first tail current source (see the tail current source 44) that is configured provide a first tail current, and wherein the first local current corresponds to a fraction of the first tail current (this is inherent the tail current 44, because the tail current 44 is the sum of all other currents at the connection node).

Regarding claim 10, wherein the fraction of the first tail current is approximately half of the first tail current (See Fig. 5 disclose the tail current source 44 is the sum the source 54 and 56, and 54 is the same as 56 therefore, the current output from 54 or 56 must be half the tail current source 44).

Regarding claim 11, Fig. 5 of an amplifier array circuit (40's, 42') with a plurality of buses (62a, 62b) for a folding analog-to-digital converter circuit, the amplifier array circuit comprising: a plurality of transconductance circuits (40's, 42's); a plurality of load circuits (62a's, 62b's), wherein each (62a, 62b) of the plurality of load circuits is separately coupled to one of the plurality of buses, wherein a first bus (62a bus) of the

plurality of buses is coupled to a portion of the plurality of transconductance circuits (40's); and a first current source circuit (54's), wherein the first current source circuit (54) is coupled to an output of a first of the portion of the plurality of transconductance circuits (output current of 40's), and wherein the first current source circuit (54's) is arranged to provide a first local current (current of 54) at the output of the first transconductance (connection node) circuit such that a maximum magnitude of current density is decreased on at least the first bus of the plurality of buses (this is inherent to Fig. 5 of Bult, because the output current of 40 is split at the output node of 40).

Regarding claim 12, wherein one of the portion of the transconductance circuits (40) is not saturated, and wherein every other transconductance circuit in the portion is saturated (42).

Regarding claim 13, Fig. 5 further comprising: another current source circuit (56) that is coupled to an output of another transconductance circuit (output of 42) in the portion of transconductance circuits.

Regarding claim 14, Fig. 5 further comprising: a plurality of current source circuits (54, 56) that includes the first current source circuit (54), wherein each of the plurality of transconductance circuits (40, 42) has an output coupled to a separate one of the plurality of current source circuits (54, 56).

Regarding claim 15. The amplifier circuit of Claim 14, wherein each of the plurality of load circuits (60a, 62a) includes a load current source (54, 56), and wherein each of the plurality of current source circuits shares a bias line (bias lines at the connection nodes) in common with one of the load current sources (54, 56).

Regarding claim 16, wherein each (40, 42) of the plurality of transconductance circuits is configured to provide a separate transconductance current on one of the plurality of buses (62a bus, 60a bus), and wherein each of the plurality of current source circuits (54, 56) is configured to supply a separate local current (current of 54, 56) such that at least a portion of the output current from each of the plurality of transconductance circuits is prevented from being carried on each of the plurality of buses (this is inherent to Fig. 5 of Bult, because the output current of 40 is split at the output node of 40).

Regarding claim 17, wherein the first transconductance circuit is configured to provide the first transconductance current in response to a differential voltage (Fig. 6); the first transconductance current is differential; and wherein the first local current is differential (Fig. 6).

Regarding claim 18, wherein the first transconductance circuit includes: a first differential pair (40, 42); and a first tail current source (44, see Fig. 4)) that is configured to provide a first tail current, and wherein the first local current corresponds to a portion of the first tail current (current tail 44 is the sum of current 54 and 56).

Regarding claim 19, wherein the portion of the first tail current is approximately half of the first tail current (See Fig. 5 disclose the tail current source 44 is the sum the source 54 and 56, and 54 is the same as 56 therefore, the current output from 54 or 56 must be half the tail current source 44).

Regarding claim 20, Fig. 5 of Bult discloses A circuit for decreasing current density on a bus (60a) coupled to a plurality of circuits (40's, 42's), the circuit

comprising: means (40) for amplifying a first input signal (input signal at the gate of 40) to provide a first current (output current of 40) to the bus; means (54) for providing a first local current; and means (connection node for canceling out at least a portion of the first current with the first local current such that a maximum magnitude of a total current on the bus is reduced (this is inherent to Fig. 5 of Bult; because the current output of 40 is split at the connected node ; therefore the current on the bus 60a is a portion of output current 40).

Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

LINH NGUYEN
PRIMARY EXAMINER

4/24/06

Art Unit 2819